

ABSTRACT

According to the invention, means for reducing the interference caused by a voltage or a current in common mode, comprise adders (S3; S4) in each path for adding a first counter-reaction voltage (V1) to the voltage of the relevant path, a bridge (R1, R2) and an inverter (I3) for provision of said first counter-reaction voltage which is equal to half the sum of the voltages (VA, VB), respectively supplied to the inputs (A; B), with an opposing sign. According to the invention, the effect of a delay introduced by the inverter (I3) may be reduced, whereby said stage further comprises means (S5; S6) for adding in addition to the input voltage for each path, a second counter-reaction voltage (Val; Vbl), and means (R1, R2, I1, S1; I2, S2) for provision of a second counter-reaction voltage (Val; Vbl) which is a function of the input voltage (VA; VB) at the input corresponding to said path, with an opposing sign and with a delay identical to that generated by the inverter (I3).